AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area.

2. (Previously Presented) A digital-analog converter circuit as claimed in claim 1, wherein each of said n analog switches comprises a conductive-type MOS transistor.

3. (Previously Presented) A digital-analog converter circuit as claimed in claim 2, wherein the n-bit digital data signal has a low amplitude equal to a reference voltage minimum less a threshold value of a P-channel MOS transistor and a high amplitude equal to a reference voltage maximum plus a threshold of an N-channel MOS transistor.

4. (Cancelled).
5. (Cancelled).
6. (Cancelled).
7. (Cancelled).
8. (Cancelled).
9. (Cancelled).

10. (Currently Amended) A liquid crystal display comprising:

a digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines,

each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area;

and a~~A~~ level shift circuit for converting a low voltage amplitude signal to a high voltage amplitude signal comprising:

a CMOS latch cell having two input sections,

wherein a first resistor element is inserted between each of the two input sections and two signal sources.

11. (Currently Amended) The liquid crystal display ~~A level shift circuit~~ as claimed in claim 10, wherein said first resistor element of said level shift circuit is a transistor.

12. (Currently Amended) The liquid crystal display ~~A level shift circuit~~ as claimed in claim 10, wherein said level shift circuit includes a second resistor element ~~the~~ is inserted between a power supply and each of the two input sections of said CMOS latch cell.

13. (Currently Amended) The liquid crystal display ~~A level shift circuit~~ as claimed in claim 12, wherein said first resistor element and said second resistor element are transistors.

14. (Currently Amended) The liquid crystal display ~~A level shift circuit~~ as claimed in claim 12, wherein level shift operation is performed only when a switch is in an on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

15. (Currently Amended) The liquid crystal display ~~A level shift circuit~~ as claimed in claim 14, wherein said level shift circuit has a control circuit to set the switch to the on status only when necessary.

16. (Currently Amended) The liquid crystal display ~~A level shift circuit~~ as claimed in claim 14, wherein said level shift circuit has a reset circuit to determine an initial status of said CMOS latch cell.

17. (Currently Amended) A liquid crystal display comprising:

a digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area;

and a~~A~~ shift register comprising a plurality of transfer stages and having a first level shift circuit to supply a start signal as a level shift to a first stage of the transfer stages and a second level shift circuit to supply a clock signal as a level shift to each of the transfer stages, wherein said first and second level shift circuits include a CMOS latch cell having two input sections and a first resistor element inserted between each of the two input sections and two input signal sources.

18. (Currently Amended) The liquid crystal display ~~A shift register~~ as claimed in claim 17, wherein said first resistor element is a transistor.

19. (Currently Amended) The liquid crystal display ~~A shift register~~ as claimed in claim 17, wherein second resistor element are inserted between a power supply and each of the two input sections of the CMOS latch cell.

20. (Currently Amended) The liquid crystal display ~~A shift register~~ as claimed in claim 19, wherein said first and said second resistor elements are transistors.

21. (Currently Amended) The liquid crystal display ~~A shift register~~ as claimed in claim 19, wherein level shift operation is performed only when a switch is in an on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

22. (Currently Amended) A shift register as claimed in claim 21, wherein said shift register has a control circuit to set said switch to the on status only when necessary.

23. (Currently Amended) The liquid crystal display ~~A shift register~~ as claimed in claim 21, wherein said shift register has a reset circuit to determine initial status of said CMOS latch cell.

24. (Currently Amended) The liquid crystal display ~~A shift register~~ as claimed in claim 17, wherein said shift register is fabricated utilizing thin firm transistors formed on a glass substrate.

25. (Currently Amended) The liquid crystal display ~~A shift register~~ as claimed in claim 17, wherein said shift register is fabricated utilizing thin film transistors formed on a silicon substrate.

26. (Cancelled).
27. (Cancelled).
28. (Cancelled).
29. (Cancelled).
30. (Cancelled).
31. (Cancelled).
32. (Cancelled).
33. (Cancelled).
34. (Cancelled).

35. (Cancelled).

36. (Cancelled).

37. (Cancelled).

38. (Cancelled).

39. (Cancelled)

40. (Currently Amended) A liquid crystal display comprising:

a digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area;

and a sampling latch circuit comprising:

a comparator configuration CMOS latch cell having two input sections;

a first switch connected between each of the two input sections and two input signal sources ;

a second switch connected between a power supply line and a power supply side of said CMOS latch cell; and

a control means to control complementary switching of said first switch and said second switch.

41. (Currently Amended) The liquid crystal display ~~A sampling latch circuit~~ as claimed in claim 40, wherein said first switch and said second switch are transistors.

42. (Currently Amended) The liquid crystal display ~~A sampling latch circuit~~ as claimed in claim 40, wherein a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuits.

43. (Currently Amended) The liquid crystal display ~~A sampling latch circuit~~ as claimed in claim 40 also having further comprising:

a third switch, synchronized and controlled by said second switch, between the power supply line and a power supply side of an output circuit for output of said CMOS latch circuit output signal.

44. (Currently Amended) The liquid crystal display ~~A sampling latch circuit~~ as claimed in claim 43, wherein said second switch is combined with said third switch.

45. (Currently Amended) The liquid crystal display ~~A sampling latch circuit~~ as claimed in claim 44, wherein a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuit.

46. (Cancelled).

47. (Cancelled).

48. (Cancelled).

49. (Cancelled).

50. (Cancelled).

51. (Cancelled).

52. (Cancelled)

53. (Cancelled)

54. (Currently Amended) A liquid crystal display comprising :

a digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area; and

~~A~~ a latch circuit including a CMOS latch cell having two input sections comprising a first switch and a second switch to respectively select a first and second power supply having different voltages and installed on at least one of a positive power side or a negative power side of said CMOS latch cell and, having control means to control switching of said first and second switches according to a latch operation period and an output operation period of said CMOS latch cell.

55. (Currently Amended) The liquid crystal display ~~A latch circuit~~ as claimed in claim 54, wherein said first and second switches are transistors.

56. (Currently Amended) The liquid crystal display ~~A latch circuit~~ as claimed in claim 54, wherein a plurality of said latch circuits are installed and, said first switch and said second switch are jointly shared by said plurality of sampling latch circuits.

57. (Currently Amended) The liquid crystal display ~~A latch circuit~~ as claimed in claim 54, wherein said latch circuit is fabricated by utilizing thin film transistors formed on a glass substrate.

58. (Currently Amended) The liquid crystal display ~~A latch circuit~~ as claimed in claim 54, wherein said latch circuit is fabricated by utilizing thin film transistors formed on a silicon substrate.